

IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) A method of forming an emitter in a vertical bipolar transistor comprising:

providing a substrate; [having a collector layer and a base layer over said collector layer, said collector layer and said base layer are formed by implantation through a single mask formed on the substrate;]

forming a single-thickness oxide over said substrate;

forming a single mask over said single-thickness oxide;

performing multiple implants through said single mask to form a base layer over a collector layer within said substrate;

forming a patterned mask over said base layer; and

filling openings in said mask with emitter material in a damascene process, said emitter material contacting the substrate.

2. (Original) The method in claim 1, wherein said substrate includes an insulator layer between a bottom silicon layer and a top silicon layer, said method further comprising:

implanting a first impurity to form said collector layer in a lower portion of said top silicon layer adjacent said insulator layer; and

implanting a second impurity to form said base layer in an upper portion of said top silicon layer.

3. (Original) The method in claim 2, wherein said emitter material includes said first impurity and said method further comprises annealing said vertical bipolar transistor to drive said first impurity into said base to create an emitter diffusion region in said base below each emitter.

4. (Original) The method in claim 2, further comprising:
patterning a second mask over said bipolar region, said mask including openings through to said base layer between adjacent ones of said emitters; and
implanting additional amounts of said second impurity into said base layer through said openings.
5. (Previously Amended) The method in claim 2, further comprising:
forming a protective layer over said emitters; and
implanting additional amounts of said first impurity into and through said insulator layer to provide a collector contact diffusion region.
6. (Previously Cancelled).
7. (Previously Amended) The method in claim 11, wherein said substrate includes an insulator layer between a bottom silicon layer and a top silicon layer, said method further comprising:
implanting a first impurity to form said collector layer in a lower portion of said top silicon layer adjacent said insulator layer; and
implanting a second impurity to form said base layer in an upper portion of said top silicon layer.
8. (Original) The method in claim 7, wherein said emitter material includes said first impurity and said method further comprises annealing said vertical bipolar transistor to drive said first impurity into said base to create an emitter diffusion region in said base below each emitter.

9. (Original) The method in claim 7, further comprising:
patterning a second mask over said bipolar region, said mask including second openings through to said base layer between adjacent ones of said emitters; and
implanting additional amounts of said second impurity into said base layer through said openings.
10. (Previously Amended) The method in claim 7, further comprising:
forming a protective layer over said emitters; and
implanting additional amounts of said first impurity into and through said insulator layer to provide a collector contact diffusion region.
11. (Currently Amended) A method of simultaneously forming complementary metal oxide semiconductor (CMOS) devices and vertical bipolar transistors on an integrated circuit chip comprising:
providing a substrate; [having a collector layer and a base layer over said collector layer, said collector layer and said base layer are formed by implantation through a single mask formed on the substrate;]
forming a single-thickness oxide over said substrate;
forming a single mask over said single-thickness oxide;
performing multiple implants through said single mask to form a base layer over a collector layer within said substrate;
forming a gate oxide layer over only said CMOS region of said SOI substrate;
forming a polysilicon layer over a CMOS region of said SOI substrate;
patterning a mask over said polysilicon layer and a bipolar region of said SOI substrate, said mask including openings over said bipolar region
depositing an emitter material in said openings in a damascene process to form emitters;
removing said mask;

patterning said polysilicon layer to form gate conductors; and
forming sidewall spacers adjacent said emitters and said gate conductors.

12. (Currently Amended) A method of simultaneously forming complementary metal oxide semiconductor (CMOS) devices and vertical bipolar transistors on an integrated circuit chip comprising:

providing a substrate; [having a collector layer and a base layer over said collector layer, said collector layer and said base layer are formed by implantation through a single mask formed on the substrate;]

forming a single-thickness oxide over said substrate;

forming a single mask over said single-thickness oxide;

performing multiple implants through said single mask to form a base layer over a collector layer within said substrate;

patterning a mask over a CMOS region and a bipolar region of said SOI substrate, said mask including first openings over said bipolar region;

depositing an emitter material in said first openings in a first damascene process to form emitters, said emitters contacting said SOI substrate;

patterning said mask to form second openings over said CMOS region;

depositing a gate conductor material in said second opening in a second damascene process to form gate conductors;

removing said mask; and

forming sidewall spacers adjacent said emitters and said gate conductors.

13. (Previously Amended) The method in claim 14, wherein said substrate includes an insulator layer between a bottom silicon layer and a top silicon layer, said method further comprising:

implanting a first impurity to form said collector layer in a lower portion of said top

silicon layer adjacent said insulator layer; and

implanting a second impurity to form said base layer in an upper portion of said top silicon layer.

14. (Currently Amended) A method of simultaneously forming complementary metal oxide semiconductor (CMOS) devices and vertical bipolar transistors on an integrated circuit chip comprising:

providing a substrate; [having a collector layer and a base layer over said collector layer, said collector layer and said base layer are formed by implantation through a single mask formed on the substrate;]

forming a single-thickness oxide over said substrate;

forming a single mask over said single-thickness oxide;

performing multiple implants through said single mask to form a base layer over a collector layer within said substrate; patterning a mask over a CMOS region and a bipolar region of said SOI substrate, said mask including first openings over said bipolar region;

depositing an emitter material in said first openings in a first damascene process to form emitters, said emitters contacting said SOI substrate;

patterning said mask to form second openings over said CMOS region;

depositing a gate conductor material in said second opening in a second damascene process to form gate conductors;

removing said mask; and

forming sidewall spacers adjacent said emitters and said gate conductors. wherein said emitter material includes said first impurity and said method further comprises annealing said vertical bipolar transistor to drive said first impurity into said base to create an emitter diffusion region in said base below each emitter.

15. (Original) The method in claim 13, further comprising:
patterning a second mask over said bipolar region, said mask including third openings through to said base layer between adjacent ones of said emitters; and
implanting additional amounts of said second impurity into said base layer through said third openings.
16. (Previously Amended) The method in claim 13, further comprising:
forming a protective layer over said emitters; and
implanting additional amounts of said first impurity into and through said insulator layer to provide a collector contact diffusion region.
17. (Previously Amended) The method in claim 14, further comprising, before said forming of said polysilicon, forming a gate oxide layer over only said CMOS region of said SOI substrate.
18. (Currently Amended) A method of forming a bipolar device on a SOI substrate having a semiconductor layer overlying a buried insulator layer to form an interface where a surface of the semiconductor layer is adjacent to a surface of the buried insulator layer, comprising the steps of:
forming a single-thickness oxide over said semiconductor layer;
forming a single mask over said single-thickness oxide;
forming in said semiconductor layer a buried collector region through said single mask,
wherein said buried collector region is centered at approximately said interface; and
forming in said semiconductor layer a base region through said single mask, wherein said base region is vertically stacked on said buried collector region,[:]
wherein said buried collector region and said base region are formed by implantation through [a] said single mask formed on the SOI substrate.
19. (Previously Cancelled).

20. (Original) The method of claim 18, further comprising:
- forming a mask having openings on the SOI substrate;
 - depositing an emitter material contacting the SOI substrate having a first impurity in said openings in a damascene process to form emitters; and
 - annealing the SOI substrate to drive said first impurity into said base region to create an emitter diffusion region in said base region below each emitter.